JC605 U.S. PTO
07/14/98

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PTO/SB/05 (1/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No	TIS-25912
First Inventor or Application Identifier	Fung Lee Chen
Title	High Density Internal Ball Grid Array
Express Mail Label No.	EM490243959 US

JC551 U.S. PTO
09/115447
07/14/98

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1 [X] * Fee Transmittal Form (e g , PTO/SB/17)
(Submit an original, and a duplicate for fee processing)

2 [X] Specification [Total Pages 36]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) (35 U S.C. 113) [Total Sheets 1]

4 Oath or Declaration [Total Pages]
a. [ ] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1 63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F R. §§ 1.63(d)(2) and 1.33(b).

5 [ ] Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6 [ ] Microfiche Computer Program (Appendix)

7 Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9 [ ] 37 C.F R §3 73(b) Statement (when there is an assignee) [ ] Power of Attorney
10 [ ] English Translation Document (if applicable)
11 [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13 [XX] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14 [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15 [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other. .....
.....

* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____
Prior application information: Examiner _____ Group / Art Unit: _____

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label (Insert Customer No or Attach bar code label here) or [ ] Correspondence address below

Name	Mark E. Courtney				
	Texas Instruments Incorporated				
Address	P.O. Box 655474, MS 3999				
City	Dallas	State	TX	Zip Code	75265
Country	USA	Telephone	972-917- 5632	Fax	972-917-4418

Name (Print/Type)	Mark E. Courtney	Registration No (Attorney/Agent)	36,491
Signature	[signature]	Date	7-14-98

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EXPRESS MAIL Mailing Label Number EM490243959 US. I hereby certify that the accompanying application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicat below and is addressed to the Ass't Commissioner of Patents, Washington, DC 20231.

By: Date:

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 790.00

Complete if Known	
Application Number	N/A
Filing Date	7-14-98
First Named Inventor	Fung Leng Chen
Examiner Name	N/A
Group / Art Unit	N/A
Attorney Docket No	TIS-25912

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

[XX] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 [ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [ ] **Payment Enclosed:** [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below		Fee Paid
Total Claims	20	-20** = 0	X	22	=	-0-
Independent Claims	3	- 3** = 0	X	82	=	-0-
Multiple Dependent				270	=	-0-

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) -0-

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Mark E. Courtney			Reg. Number	36,491
Signature		Date	7-14-98	Deposit Account User ID	---

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HIGH DENSITY INTERNAL BALL GRID ARRAY INTEGRATED CIRCUIT PACKAGE

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to the field of integrated circuit packages and more specifically to substantially flat integrated circuit packages having multiple slots around the perimeter of the substrate for wire bonding and attachment of a silicon chip and having a ball grid array disposed on the substrate internal of the multiple slots.

BACKGROUND OF THE INVENTION

Without limiting the scope of the invention, its background is described in connection with integrated circuit packages, as an example.

Heretofore, in this field, integrated circuits have been formed on semiconductor wafers. The wafers are separated into individual chips and the individual chips are then handled and packaged. The packaging process is one of the most critical steps in the integrated circuit fabrication process, both from the point of view of cost and of reliability. Specifically, the packaging cost can easily exceed the cost of the integrated circuit chip and the majority of device failures are packaging related.

The integrated circuit must be packaged in a suitable media that will protect it in subsequent manufacturing steps and from the environment of its intended application. Wire bonding and encapsulation are the two main steps in the packaging process. Wire bonding connects the leads from the chip to the terminals of the package. The terminals allow the integrated circuit package to be connected to other

components. Following wire bonding, encapsulation is employed to seal the surfaces from moisture and contamination and to protect the wire bonding and other components from corrosion and mechanical shock.

Conventionally, the packaging of integrated circuits has involved attaching an individual chip to a lead frame, where, following wire bonding and encapsulation, designated parts of the lead frame become the terminals of the package. The packaging of integrated circuits has also involved the placement of chips on a flexible board where, following adhesion of the chip to the surface of the flexible board and wire bonding, an encapsulant is placed over the chip and the adjacent flexible board to seal and protect the chip and other components.

Unfortunately, current methods for encapsulating silicon chips have led to various problems, including cracking between the encapsulation material and the integrated circuit components, as well as high failure rates due to the multi-step nature of the process. Cracking has plagued the industry because of differences in the coefficient of thermal expansion

of the different components, for example, between the soldering materials at the different interfaces and between metallic and non-metallic components. Cracking is also frequent between the silicon wafer and the encapsulation materials, usually epoxies, due to the extreme variations in temperature in various environments and between periods of operation and non-operation.

Even if the encapsulated silicon chip is successfully assembled into a working integrated circuit, another problem is commonly encountered. Once the silicon chip is encapsulated it is typically surface mounted using radiant heat or vapor saturated heating. This process, however, can lead to poor coplanarity due to uneven reflow, leading to integrated circuit failure.

Therefore, a need has arisen for an integrated circuit package and a process for producing an integrated circuit package that provides for minimizing the size of integrated circuit packages. A need has also arisen for an integrated circuit package that allows for wire bonding of the silicon chip to the printed circuit board around the perimeter of the

printed circuit board while providing maximum protection to the critical components of the integrated circuit package. Also, a need has arisen for an integrated circuit package that utilizes the surface area toward the center of the printed circuit board for attachment of a high density ball grid array. Finally, a need has arisen for an integrated circuit package that solves the problem caused by the differences in thermal expansion of the packaging materials and does not require extensive encapsulation.

SUMMARY OF THE INVENTION

The present invention disclosed herein comprises an integrated circuit package that utilizes slots around the perimeter of the substrate for wire bonding the silicon c hip to the substrate. The integrated circuit package of the present invention also utilizes the region of the printed circuit board inside the slots for locating a high density ball grid array. The present invention reduced the differences in the coefficient of thermal expansion of the packaging components by having a substrate with multiple opening filled with potting material.

The integrated circuit package comprises a substrate having two or more openings disposed proximate the perimeter of the substrate, first and second surfaces and an outline. A plurality of routing strips are integral with the substrate. A plurality of pads are centrally disposed on the first surface, at least one of the pads being electrically connected with at least one of the routing strips. A chip is adhered to the second surface of the substrate. The chip has an outline that is less than the outline of the substrate. The chip has

at least one bonding pad, which serves to provide electrical connections to the substrate. Wire bonding electrically connects the bonding pad to the routing strips through the openings on the substrate. The wire bonding is protected from the environment by a potting material that is disposed within the openings in the substrate.

The chip is adhered to the substrate by the potting material that may be, for example, polyimide. Alternatively, the chip may be adhered by an adhesive layer, such as a polyimide adhesive layer or an adhesive epoxy tape. The epoxy can either be coated on the surface of the substrate or the chip prior to assembly.

Solder balls are disposed on the pads of the first surface of the substrate to enable attachment to other devices. The solder balls may preferably have a diameter between about 8 and 20 mils. The chip may preferably have a thickness between about 10 and 20 mils. In one embodiment, potting material encapsulates the chip adding a thickness of about 6 mils. The substrate may preferably have a thickness

between about 8 and 28 mils. In a single layer embodiment, the substrate has a thickness of about 12 mils.

In a multi-layer embodiment, the integrated circuit package of the present invention has bus bars and routing strips are disposed adjacent to the openings of the substrate. The first layer may have a thickness of about 12 mils and a second layer may have a thickness of about 8 mils. Alternatively, a first layer may have a thickness of about 12 mils, a second layer may have a thickness of about 8 mils and a third layer may have a thickness of about 8 mils. The profile of the integrated circuit package of the present invention may preferably be between about 30 mils and 50 mils.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

Figure 1 is a simplified top view of an integrated circuit package of the present invention; and

Figure 2 is a simplified end cross-sectional view of an integrated circuit package of the present invention along the A-A' line of figure 1.

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention.

The present invention is related to high frequency integrated circuit packages having both a low profile and a small outline. As defined herein, the term "outline" relates to the overall width and length of, for example, the entire integrated circuit package of the present invention. The outline of the integrated circuit package is also referred to as the footprint of the integrated circuit package, because it defines the surface area on a motherboard that the integrated circuit package will occupy. Outline may be measured, in for example, square mils or square millimeters.

As defined herein, the term "profile" refers to thickness or height of, for example, the integrated circuit package of the present invention. The integrated circuit package of the present invention may be measured in, for example, mils. As defined herein, the term "substantially similar" refers to the relative outlines of the printed circuit board and the silicon chip, which are within less about 10% of one another other. In one embodiment of the present invention, the difference in the outlines is about 2%. In an alternative embodiment, the silicon chip and the printed circuit board have the same outlines. Importantly, the term substantially similar does not indicate which of the two components is larger, as either form is encompassed by the present invention.

The present invention provides for an integrated circuit package that delivers high speed performance and meets the space constraint requirements of modern semiconductors. The present invention also addresses the problems associated with the electronic capacity of the chip assembly. The principles of the present invention may be incorporated into, for example, a synchronous DRAM (SDRAM) silicon chip. However,

the present invention is also applicable to LOGIC, SRAM, EPROM and any other integrated circuit components.

Figure 1 is a top view depicting the outline of an integrated circuit package 30 of the present invention. A printed circuit board 70 is depicted having openings 86 around the perimeter of printed circuit board 70. The number of openings 86 may be varied up or down depending on design or assembly constraints such as the thickness, width, length, coefficient of thermal expansion and composition of the printed circuit board 70. Pads 100 are centrally located on the printed circuit board 70 and are connected to routing strips 82 by conduits and vias (not depicted) within the printed circuit board 70. The silicon chip 50 has bonding pads 120 located generally in the outer areas of silicon chip 50 surrounding the periphery of the silicon chip 50. Bonding pads 120 are connected to routing strips 82 of printed circuit board 70 by wire bonding 80.

The printed circuit board 70 of the present invention may be varied in thickness to allow more flexibility than conventional printed circuit boards 70. The increased

flexibility allows the printed circuit board 70 of the present invention to more closely match the movement and expansion of the silicon chip 50. By filling the openings 86 with a potting material 90 that closely matches the coefficient of thermal expansion of the silicon chip 50 or the printed circuit board 70, or both, stress caused by thermal expansion on the components is reduced. Reduced stress on the components increases the yield during packaging, and also increases device reliability and endurance.

Bus-bars (not depicted) may be included in the printed circuit board 70. The bus bars may serve, for example, as power supplies or grounds, and it is preferred that one bus bar serve one function, such as a power supply, and a second bus bar serve another function, such as a ground.

Figure 2 is a simplified cross-sectional view of an integrated circuit package taken along the A-A' line depicted in figure 1 that is generally designated 30. The integrated circuit package 30 comprises a silicon chip 50, which can be, for example, any integrated circuit component such as a DRAM, an EPROM, a SRAM or a LOGIC chip. A printed circuit board 70

is attached to the silicon chip 50 by the potting material 90. If necessary, an adhesive layer (not depicted) may be placed between the printed circuit board 70 and the silicon chip 50. The printed circuit board 70 depicted has two layers, a top layer 76 and a bottom layer 78.

It should be understood by one skilled in the art that the terms "top" and "bottom" as well as the terms "side" and "end" are used for illustration purposes only, as the integrated circuit package 30 of the present invention can be assembled and used in a variety of positions and ways.

The printed circuit board 70 may be constructed from a material such as FR-4, FR-5 or BR. FR-4, for example, is available from Motorola Inc., U.S.A., and is an epoxy resin reinforced with a woven glass cloth. In selecting the material for printed circuit board 70, one skilled in the art will recognize that four parameters should be considered, namely: thickness, dielectric constant, glass transition temperature and the coefficient of thermal expansion.

The thickness of top layer 76 and bottom layer 78 is dependant on the number of layers required to electrically

connect bonding pads 120 on silicon chip 50 and the pads 100 on the first surface 92 of the printed circuit board 70. The thickness of the layers will also depend on the amount of reinforcement required in a given layer. The reinforcing glass cloth can range in thickness from 2 mil per sheet (type 106) to about 8 mil per sheet (type 7628). Dielectric constant is determined by a combination of the resin used and the thickness and type of reinforcement used. Standard FR-4 has a dielectric constant of about 4.5. The dielectric constant can be reduced to about 3 by replacing the epoxy resin with a cyanate ester resin. The greater the thickness, however, the greater the problems associated with thickness control, rough surfaces, excessive drill reflection and poor resin refill.

The temperature at which a resin changes from a glass-like state into a "rubbery" state is generally designated as T_g. Standard FR-4 is made with a bifunctionally polymerizing epoxy that has a T_g of about 110 °C. Higher T_g temperatures, such as 125-150 °C may be withstood by using a tetrafunctional epoxy. For higher T_g values, in the range of 150 to 200 °C a

cyanate ester:epoxy blend can be used. Additionally, polyimides provide for printed circuit boards having a T_g above 250 °C.

The coefficient of thermal expansion for FR-4 is about 16 ppm/°C. A difference in the coefficient of thermal expansion between the printed circuit board 70 made from FR-4 and the silicon chip 50 can lead to failure of the integrated circuit package 30 during, not only the assembly of the integrated circuit package 30, but also during its use.

Solder balls 150 are used with the present invention, and may be attached to the pads 100 forming a high density ball grid array in the center of printed circuit board 70. A conventional solder reflow system, for example, a vapor phase solder reflow system may be used to attach solder balls 150 to pads 100. In this system, condensed vapor surrounds the integrated circuit package 30 and the printed circuit board 70 with a cloud of steam. A liquid, such as a nonchlorinated (non CFC) fluorocarbon is first heated with enough energy to form a vapor and to sustain a vapor cloud. When the integrated circuit package 30 is then passed through the

vapor, the vaporized liquid condenses thereon and gives off the latent heat of vaporization. This energy is then transferred to the integrated circuit package 30. As long as the integrated circuit package 30 remains in the vapor, the vapor continues to give off energy at a repeatable fixed rate and temperature, until the integrated circuit package 30 reaches the temperature of the vapor.

The advantage of using a nonchlorinated fluorocarbon is that it is extremely thermally stable, colorless, odorless and nonflammable. In addition, it has a low toxicity, low surface temperature, low boiling point, and low heat of vaporization. Because the fluid form of the non-chlorinated fluorocarbon is inert, it does not react with fluxes or component materials, nor does it absorb oxygen or other gases that cause reactions during the solder reflow. Most commercially available fluorocarbons used for vapor phase reflow are formulated to vaporize at precisely stable reflow temperatures for different solder materials, as will be known to those skilled in the art.

The vaporization temperature will depend on the solder type being used. A brief list of the temperatures for reflux of non-chlorinated fluorocarbons and the composition of the solder types that are used is shown below.

Vaporization Temperatures and Solder Types

Fluid Temperature	Solder Type
56, 80, 97, 101, 102°C and 155°C	100 In 37 Sn/38 Pb/25 In
165°C	70 Sn/18 Pn/12 In 70 In/30 Pb
174°C	60 In/40 Pb
190°C	90 In/10 Ag 50 In/50 Pb 63 Sn/37 Pb 70 Sn/30 Pb 60 Sn/40 Pb
215°C and 230°C	60 Sn/40 In 60 Sn/40 Pb 63 Sn/37 Pb 70 Sn/30 Pb 62 Sn/36 Pb/2 Ag
240°C and 253°C	75 Pb/25 In 81 Pb/19 In
260°C and 265°C	96.5 Sn/3.5 Ag

Alternatively, infrared or radiant heated solder reflow may be used to place solder balls 150 on pads 100. In such a system each component of the soldering system is directly exposed to radiation from a heating element. Heat from the radiant energy element is absorbed by the different components

according to its molecular structure, leading to bonding between the pads 100 and solder balls 150.

Conventional radiant heat systems expose only the outer surfaces of the components to the radiant heat, which may not reach interior areas as efficiently as with vapor saturated heating methods as described above. The present invention, however, is not affected by this typical problem because of the use of solder balls 150 instead of leads. In fact, due to the reduced overall size either method, vapor phase solder reflow or radiant heated solder reflow, may be effectively used with the present invention.

The multi-slot printed circuit board 70 of the present invention also solves other problems associated with solder reflow systems. These problems include the creation or failure due to voids, coplanarity, tombstoning, open joints, component cracking, thermal shock and thermal stressing. The present invention solves these problems because the potting material 90 serves to attach the printed circuit board 70 to silicon chip 50. The multi-slot printed circuit board 70 also

dispenses with the need for electrically connecting soldering leads to the integrated circuit package 30.

By using solder balls 150 instead of leads, the problems associated with voids around pad areas or under leads caused by incomplete reflow or poor welding of the soldering surface due to improper flux or badly oxidized surfaces is eliminated. The problems of coplanarity and tombstoning are also reduced or eliminated using the solder balls 150 because surface tension on both sides of the solder balls 150 is equal.

Even though Figure 2 depicts printed circuit board 70 as having two layers, top layer 76 and bottom layer 78, it should be understood by one skilled in the art that printed circuit board 70 may consist of a single layer or may be a multi-layered board having an alternate number of layers. Furthermore, figure 2 shows a conduit 118 connecting routing strip 82 to via 84. In one alternative embodiment, via 84 connects directly to routing strip 82 without a need for conduit 118. Conduit 118, however, may be useful for connecting together a plurality of pads 100 or routing strips 82.

The above described components and their constructions and interrelation provide an assembly that is encapsulated as described below. The term "assembly" refers to the assembled components prior to encapsulation. The assembly consists of printed circuit board 70, a silicon chip 50 and wire bonding 80. The printed circuit board 70 has openings 86 with routing strips 82 and bus bars extending into, or to, the openings 86. Disposed on the upper surface 92 of printed circuit board 70, and more specifically top layer 76, are pads 100 on which solder balls 150 or solder columns are positioned for providing electrical connection to a mother- or sister-board.

The wire bonding 80 process may begin after silicon chip 50 has been adhered to printed circuit board 70. Silicon chip 50 and printed circuit board 70 are then positioned on a heated pedestal to raise the temperature of the combination to a point between 100°-300°C. A gold wire having a diameter typically ranging from 0.7 mil. to 1.3 mil. is strung through a heated capillary where the temperature may range between 200°-500°C. A soldering ball is created at the end of the wire using either a flame or a spark technique. This

soldering ball is then brought to bonding pad 120 on the silicon chip 50 and a combination of compression force and ultrasonic energy are used to create the desired metallurgical bond.

Using this "stitch" technique significantly reduces the cross-section of the wire at that point. A loop is created in the wire bonding 80 above the bond that has just been achieved, and the wire bonding 80 is routed to the desired connection on the printed circuit board 70 such as routing strip 82 or bus bar. The wire bonding 80 is clamped and the capillary raised, such that the wire bonding 80 will break free at the outer edge of the bond. This process is repeated until all the bonding pads 120 that require electrical connection on the silicon chip 50 are electrically connected to printed circuit board 70.

Following the assembly of the above-described components, the openings 86 are filled with potting material 90. The potting material 90 may attach the printed circuit board 70 to the silicon chip 50 if an adhesive layer is not disposed between the printed circuit board 70 and the silicon chip 50.

The potting material 90 fills the openings 86 and protects the wire bonding 80 from the environment. The potting material 90 also helps protect the wire bonding 80 from mechanical stress, and provides mechanical support. By using potting material 90 to fill the openings 86 and protect the wire bonding 80, the integrated circuit package 30 of the present invention may be produced with less steps and has decreases warpage caused by the use of the potting materials 90 to adhere and encapsulate the component of the integrated circuit package 30. By using a printed circuit board 70 having a plurality of openings 86, the printed circuit board is exposed to less stress than in conventionally potted and encapsulated integrated circuit packaging because the potting material 90 can be selected to more closely match the coefficient of thermal expansion of the printed circuit board 70 and the silicon chip 50.

The potting material 90 may be a cyanate ester-type resin available from Shin-Etsu Chemical Co., Ltd., such as KMC 184VA and KMC 188VA-4. Other examples of potting materials 90 that may be used with the present invention include epoxies, polyesters, polyimides, cyanoacrylates, ceramic, silicone and

urethane. The potting materials 90 may also contain fillers that affect the coefficient of thermal expansion, as well as the strength and flexibility of the potting material 90. The selection of potting material 90 and fillers will depend on the components used to make the integrated circuit package 30, as will be known to those of skill in the art.

Docket No. 9404

Properties of Typical Potting Resins

	Epoxy	Polyester	Silicone	Urethane
Dielectric constant, D-150				
60 Hz	3.9	4.7	2.7	5.7
10^6 Hz	3.2	---	2.7	3.4
Dissipation factor, D-150				
60 Hz	0.04	0.017	0.001	0.123
10^6 Hz	0.03	---	0.001	0.03
Dielectric strength, D-149; V/mil	450	325	550	400
Volume resistivity, D-257; $\Omega \cdot cm$	10^{15}	10^{14}	10^{15}	10^{13}
Arc resistance, D-495; seconds	150	135	120	180
Specific gravity, D-792	1.15	1.2	1.05	1.0
Water absorption, D-570; % 24 h	0.15	0.3	0.12	0.4
Heat deflection temperature, D-648; at 264 lb/in^2, °F	380	260	< 70	< 70
Tensile strength, D-638; lb/in^2	9000	10,000	1000	2000
Impact strength (Izod), D-256; ft · lb/in	0.5	0.3	No break	No break
Coefficient of thermal expansion, D-969; 10^{-5}/°F	5.5	7.5	4.0	15
Thermal conductivity, C-177; Btu · in/($h \cdot ft^2 \cdot$°F)	1.7	1.7	1.5	1.5
Linear shrinkage; %	0.3	3.0	0.4	2.0
Elongation, D-638; %	3	3	175	300

The present invention, therefore, is directed toward an integrated circuit package 30 having openings 86 around the perimeter of printed circuit board 70 allowing for a high density ball grid array to be disposed around the center of

printed circuit board 70 while having an overall reduction in outline and profile. The present invention also allows for decreased failure due to the reduced number of soldered materials having varying coefficients of thermal expansion. The present invention further reduces the overall number of steps in the assembly of, for example, memory units by streamlining the assembly process not only in reduced number of steps, but also by elimination the curing steps associated with a potting step followed by an encapsulation step. The present invention further reduces the amount of material, and the types of materials used in producing integrated circuit packages 30, thereby saving time, money and the environment.

Furthermore, the present invention takes advantage of the openings 86 in the printed circuit board 70 for potting the wire bonding 80 that connects the silicon chip 50 and the printed circuit board 70 in a single step, and to decrease the stress caused by varying coefficients of thermal expansion. By filling the openings 86 with potting material 90, the wire bonding 80 between silicon chip 50 and the printed circuit board 70 is generally protected from the environment in

general, and more particularly, protected from moisture due to the hermetic nature of the encapsulation. By filling the openings 86, the integrated circuit package 30 of the present invention minimizes warpage caused by the differences in the coefficients of thermal expansion between the printed circuit board 70 and the silicon chip 50.

The potting and encapsulation of the integrated circuit package 30 of the present invention as described herein also reduces the overall profile by allowing the non-operative or backside of the silicon chip 50 to be exposed. A smaller profile is achieved while at the same time providing for hermetical protecting of the connections between the silicon chip 50 and the printed circuit board 70, at the openings 86. Additionally, reduced environmental impact is obtained using the apparatus of the present invention due to the overall decrease in the size of the integrated circuit package 30.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other

embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

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What is claimed is:

1. An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a chip adhered to said second surface of said substrate;

a plurality of pads disposed on said first surface of said substrate generally centralized within said peripheral openings of said substrate; and

potting material filling said peripheral openings.

2. The integrated circuit package as recited in claim 1 wherein said substrate has a first and a second layer.

3. The integrated circuit package as recited in claim 1 further comprising a plurality of routing strips being integral with said substrate.

4. The integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said first

surface of said substrate is electrically connected with at least one of said routing strips.

5. The integrated circuit package as recited in claim 1 further comprising at least one solder ball disposed on one of said pads.

6. The integrated circuit package as recited in claim 1 further comprising a plurality of solder balls disposed on said pads forming a high density ball grid array.

7. The integrated circuit package as recited in claim 1 wherein said potting material adheres said chip to said substrate.

8. An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed centrally on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads adhered to said second surface of said substrate; and

wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips.

9. The integrated circuit package as recited in claim 8 further comprising at least one solder ball disposed on one of said pads.

10. The integrated circuit package as recited in claim 9 wherein said at least one solder ball is between about 8 and 20 mils in diameter.

11. The integrated circuit package as recited in claim 8 further comprising a plurality of solder balls disposed on said pads forming a high density ball grid array.

12. The integrated circuit package as recited in claim 8 wherein said chip has a thickness between about 10 and 20 mils.

13. The integrated circuit package as recited in claim 8 wherein said substrate has a thickness of between about 8 and 28 mils.

14. The integrated circuit package as recited in claim 8 wherein said substrate has first and second layers and wherein said first layer has a thickness of about 12 mils and said second layer has a thickness of about 8 mils.

15. The integrated circuit package as recited in claim 6 wherein said substrate has first, second and third layers and wherein said first layer has a thickness of about 12 mils, said second layer has a thickness of about 8 mils and said third layer has a thickness of about 8 mils.

16. An integrated circuit package comprising:

a substrate having a plurality of peripheral openings, first and second surfaces and an outline;

a plurality of routing strips being integral with said substrate;

a plurality of pads centrally disposed on said first surface at least one of said pads being electrically connected with said routing strips;

a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate and having a plurality of bonding pads;

wire bonding electrically connecting said bonding pads to said routing strips;

vias connecting said routing strips to said pads;

potting material filling said peripheral openings and covering said wire bonding and said bonding pads; and

a plurality of solder balls centrally disposed on said pads disposed on said first surface of said substrate forming a high density ball grid array.

17. The integrated circuit package as recited in claim 16 wherein said chip has a thickness between about 10 and 20 mils.

18. The integrated circuit package as recited in claim 16 wherein said substrate has a thickness of between about 8 and 28 mils.

19. The integrated circuit package as recited in claim 16 wherein said substrate has first and second layers and wherein said first layer has a thickness of about 12 mils and said second layer has a thickness of about 8 mils.

20. The integrated circuit package as recited in claim 16 wherein said substrate has first, second and third layers and wherein said first layer has a thickness of about 12 mils, said second layer has a thickness of about 8 mils and said third layer has a thickness of about 8 mils.

HIGH DENSITY INTERNAL BALL GRID ARRAY INTEGRATED CIRCUIT PACKAGE

ABSTRACT OF THE DISCLOSURE

An integrated circuit package (30) comprising a substrate (70) having peripheral openings (86) and first and second surfaces (92, 94), a plurality of routing strips (82) being integral with the substrate (70), a plurality of pads (100) centrally disposed on the first surface (92) and electrically connected with at least one of the routing strips (82), a chip (50) having bonding pads (120) adhered to the second surface (84) of the substrate (70), wire bonding (80) electrically connecting at least one bonding pad (120) to at least one of the routing strips (82) and potting material (90) filling the openings (86) to adhere the chip (50) to the substrate (70) and surrounding the wire bonding (80), is disclosed.

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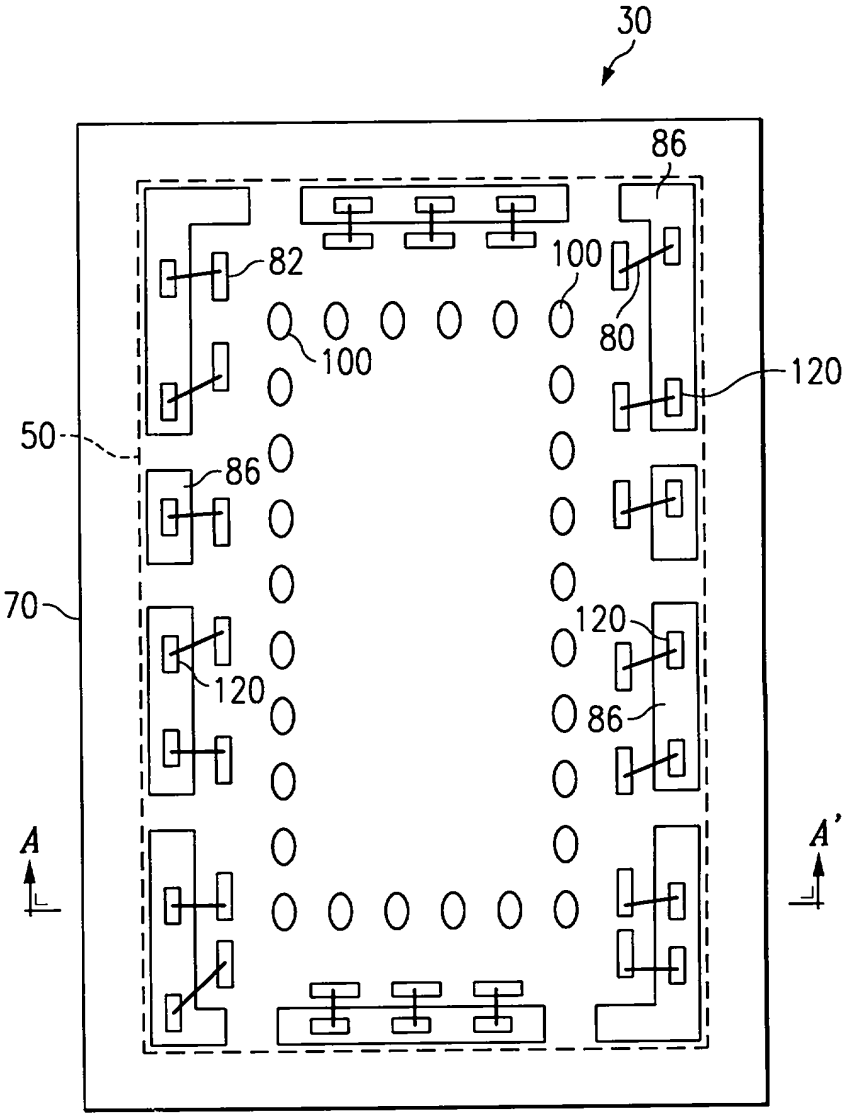
30
86
82
100
100
80
120
50
86
70
120
120
86
A
A'

FIG. 1

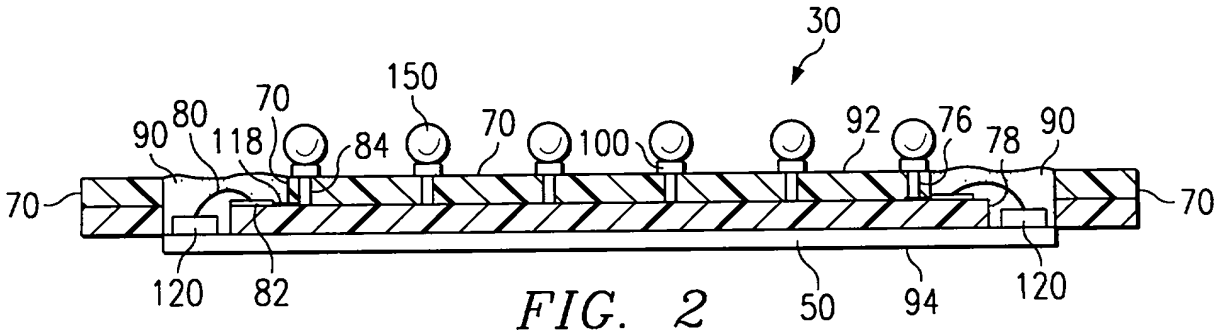
30
150
70
90
80
118
84
70
100
92
76
78
90
70
70
120
82
50
94
120

FIG. 2

TI Docket No.
TIS-25912

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: High Density Internal Ball Grid Array Integrated Circuit Package

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Robby T. Holland, Reg. No. 33,304; W. James Brady III, Reg. No. 32,080; Alan T. Stewart, Reg. No. 35,373; Warren L. Franz, Reg. No. 28,716; Mark E. Courtney, Reg. No. 36,491; Rose A. Keagy, Reg. No. 35,095 W. Daniel Swayze Jr., Reg. No. 34,478; Jay M. Cantor, Reg. No. 19,906

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Mark E. Courtney Texas Instruments Incorporated Mail Station 3999 P.O. Box 655474 Dallas, TX 75265	Mark E. Courtney (972) 917-5632 (972) 917-4418 Fax

NAME OF INVENTOR: (1)	NAME OF INVENTOR: (2)	NAME OF INVENTOR: (3)
Fung Leng Chen	Chee Kiang Yew	Pang Hup Ong
RESIDENCE & POST OFFICE ADDRESS: 36 West Coast Place Singapore 127588	RESIDENCE & POST OFFICE ADDRESS: Blk 866, #04-313 Woodlands St. 83 Singapore 730866	RESIDENCE & POST OFFICE ADDRESS: 49 Jalan Peliti Singapore 537340
COUNTRY OF CITIZENSHIP: Singapore	COUNTRY OF CITIZENSHIP: Singapore	COUNTRY OF CITIZENSHIP: Singapore
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE:	DATE:	DATE: